I claim:

1. A controller capable of determining when a system reaches a maximum allowable energy, J_{max}, the controller comprising:

means for monitoring the power, W, in the system at fixed average time intervals, Δt;

for each time interval, summing in a register, a digital number corresponding to the power during that time interval;

comparing the sum in the register to a value, B, where B represents the maximum allowable energy, J_{max}, divided by the fixed, average time interval, $(B = J_{max}/\Delta t)$, and

a means for generating a control signal when the sum in the register reaches B.

2. A power controller capable of determining when a system reaches a maximum allowable energy, comprising means for:

digitally monitoring a current, I, at fixed, average intervals, Δt;

obtaining the square of the current, I^2;

subtracting the square of the rated, current-carrying capacity of the system, I_o^2;

summing the values of $(I^2 - I_o^2)$ in a first register, the values in the first register always being greater than or equal to zero;

comparing the sum in the first register to a first control value, K_t, where K_t is equal to the rectilinear hyperbola constant, K, of a constant energy plot of percent rated current as a function of time, (Fig. 1), divided by the fixed average interval, $K_t = K/\Delta t$, and

a means for sending a control signal when the value in the first register equals or exceeds the first control value, K_t.

3. A power controller according to claim 2, wherein the controller is implemented in a device selected from a group consisting of Programmable Array Logic (PAL), Programmable Logic Devices (PLD), Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC).

4. A power controller according to claim 2, wherein the controller is implemented in a device selected from a group consisting of Digital Signal Processors (DSP), microcontrollers and microprocessors.

5. A power controller according to claim 2, further comprising means for instantaneous shutdown.

6. A power controller according to claim 2, further comprising means for current limiting.

7. A power controller according to claim 2, further comprising a means for foldback current limiting.

8. A solid state power controller according to claim 2, further comprising a means for monitoring energy in a solid state switch, and comparing it to a safe operating area, SOA, of the solid state switch, the solid state power controller comprising means for:

measuring voltage across the solid switch, E, for each fixed average time interval, Δt;

subtracting from the measured voltage, E, a predetermined, safe threshold voltage, E_t,

$\Delta E = E - E_t$;

determining the product of the current times the difference between the voltage and the safe threshold voltage, $I \bullet \Delta E$, for each fixed average time interval;

summing the values of $I \bullet \Delta E$ in a second register; the values in the second register always being greater than or equal to zero;

comparing the sum in the second register to a second control value, C_t, said second value representing the safe operating limit of the solid state switch, $\int((E-E_t)I)dt$, divided by the fixed average interval, Δt, $C_t = (\int((E-E_t)I)dt)/\Delta t$, and

sending a control signal when the sum in the second register equals or exceeds the second value, C_t.

9. A solid state power controller according to claim 8, further comprising means for instantaneous shutdown

10. A solid state power controller according to claim 8, further comprising means for current limiting.

11. A solid state power controller according to claim 8, further comprising a means for foldback current limiting.

12. A solid state power controller according to claim 8, wherein the controller is implemented in a device selected from a group consisting of Programmable Array Logic (PAL),

Programmable Logic Devices (PLD), Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC).

13. A solid state power controller according to claim 8, wherein the controller is implemented in a device selected from a group consisting of Digital Signal Processors (DSP), microcontrollers and microprocessors.

14. A controller for monitoring the energy in a solid state switch, and comparing it to a safe operating area, SOA, of the solid state switch, comprising means for:

measuring the voltage across the solid state switch, E, and the current flowing through the solid state switch, I, at fixed average time intervals, Δt;

subtracting from the measured voltage, E, a predetermined, safe threshold voltage, E_t, obtaining the difference, $\Delta E = E - E_t$;

determining the product of the current times the difference, $I \bullet \Delta E$, for each fixed average time interval;

summing the values of $I \bullet \Delta E$ in a register; the values in the register always being greater than or equal to zero;

comparing the sum in the second register to a value, C_t, said value representing the safe operating limit of the solid state switch, $\int((E-E_t)I)dt$, divided by the fixed average time interval, Δt, $C_t = (\int((E-E_t)I)dt)/\Delta t$, and

sending a control signal when the sum in the second register exceeds the control value, C_t.

15. A solid state power controller according to claim 14, further comprising means for instantaneous shutdown

16. A solid state power controller according to claim 14, further comprising means for current limiting.

17. A solid state power controller according to claim 14, further comprising a means for foldback current limiting.

18. A solid state power controller according to claim 14, wherein the controller is implemented in a device selected from a group consisting of Programmable Array Logic (PAL), Programmable Logic Devices (PLD), Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC).

19. A solid state power controller according to claim 14, wherein the controller is implemented in a device selected from a group consisting of Digital Signal Processors (DSP), microcontrollers and microprocessors.

20. In a controller having an algorithm for an I^2t overload trip function wherein the algorithm creates a signal when the integral with respect to time of the square of the current (I^2) minus the square of the rated current (I_o^2) reaches an I^2t overload value, $\int(I^2-I_o^2)dt=K$, the simplified algorithm characterized by:

digitally sampling the current at fixed intervals, Δt; summing the square of the sampled current minus the square of the rated current in a first register, the register never being allowed to go below zero, and creating a signal when the sum in the first register is equal or greater than the overload value divided by the current sampling interval, $K/\Delta t$.

21. A controller according to claim 20, further comprising a simplified algorithm for monitoring the energy in a solid state switch and comparing the energy to a safe operating area of a solid state switch characterized by:

digitally sampling the voltage across the solid state switch at the fixed time interval; subtracting a digital value of a predetermined safe, threshold voltage from the sampled voltage; multiplying the voltage difference and sampled current together; summing the products of the multiplications in a second register, the second register never being allowed to go below zero, and when the sum in the second register reaches a predetermined safe operating area limit, generating a control signal.

22. A controller comprising a simplified algorithm for monitoring the energy in a solid state switch and comparing it to a safe operating area of a solid state switch characterized by:

digitally sampling the voltage across the solid state switch at a fixed time interval; subtracting a digital value for a predetermined safe, threshold voltage from the sampled voltage; multiplying the sampled current and voltage difference together; summing the products of the multiplications in a register, the register never being allowed to go below zero, and when the

sum in the register reaches the predetermined safe operating area limit, generating a control signal.